In the Drawings

Applicants respectfully acknowledge the Examiner's indication that the proposed drawings submitted with Applicants' Reply and Amendment dated October 20, 2005 have been accepted.

Remarks

Claims 1-11 are pending in the application. Claims 1-8 and 11 stand rejected and claims 9 and 10 are objected to. By this amendment claims 9-11 have been amended; claim 8 has been canceled; and new claim 12 has been added. Applicants respectfully request reconsideration of all pending claims herein.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner rejected claim 1-8 and 11 under 35 U.S.C. § 102(b) as being anticipated by U.S Patent No. 5,672,987 to Tanaka. The Examiner stated that Tanaka discloses various elements corresponding to the limitations of Applicants' structure recited in independent claim 8, citing Tanaka at Col. 5, lines 19-23, lines 58-67 and Col. 6, lines 1-37 and 58-67.

Applicants respectfully submit that Tanaka is directed to a method of reducing the cycle time of a pipelined memory array by inserting a "potential difference transmission circuit" between a memory array and a sense amplifier to restrain the amplitude of a sensed differential bit line pair. (Tanaka, Col. 3, lines 16-32.) Tanaka's potential difference transmission circuit holds the potential difference between a pair of bit lines and transmits this potential difference to the next pipeline stage of the memory. (Col. 3, lines 19-24). With this structure, Tanaka teaches that the overall cycle time of a pipelined memory array may be reduced.

Conversely, Applicants' method is directed to reducing power dissipation from unnecessary precharging of memory bitlines following a write access. In other words, Applicants' method contemplates precharging the bitlines of the memory only when a read access follows the current access operation. (Applicants' Specification at paragraph 11, claim 1.) When a write access follows the current access operation, Applicants' precharge circuitry is disabled. (Applicants' Specification at paragraph 11, claim 1.) As such, Applicants respectfully submit that the method claimed herein is not anticipated or suggested by Tanaka.

The Examiner cited the operation of Tanaka's timing control circuit at Col 5, lines 19-23, which merely observes that a bit line precharge operation is timing driven event, i.e.: "The precharge enable signal PRB is used to define the time at which the precharge circuit precharges the pair of bit lines BL and XBL." Similarly, the text cited by the Examiner at Col. 6, lines 1-37 references "...the operation of Tanaka's memory for the case where the data at a "Low" level is stored in the memory cell 100 is described as an example." (Tanaka at Col. 6, lines 8-10) Applicant's respectfully submit the text cited by the Examiner does not anticipate or suggest a method for limiting the bit line precharge to when the next memory access will be a read access. Indeed, Tanaka does not disclose nor claim a memory array having a read cycle signal controller for generating a read cycle (n+1) signal when a next memory access operation is a read access operation, nor does Tanaka logically evaluate the first precharge control signal and the read cycle control (n+1) signal to determine whether a next memory access is a read access operation for gating the precharge circuit. (Applicants' Specification, paragraphs 11-13, claim 8.)

In addition, Applicants' describe a mode of operation in which the latency required to evaluate whether the n+1 cycle will be a read access is generated by adding an extra clock cycle to the memory access time. (Applicants' Specification at paragraph 30, claim 7.) As such, the methodology claimed by Applicants emphasizes the stated objective of saving power at the expense of performance, which is similarly not anticipated by Tanaka.

The Examiner rejected Claims 1-7, stating that the rejected apparatus of claim 8 would perform the recited method of claims 1-7 and citing Fig. 3 of Tanaka. However, contrary to Applicants' claimed method, Fig. 3 of Tanaka shows a precharge operation occurring immediately prior to a write access operation between t_4 and t_5, and therefore Tanaka teaches away from Applicants' method.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Tanaka does not teach or suggest Applicants' method of limiting bit line

precharge to access operations in which the next access operation is a read access. Similarly, Tanaka does not anticipate the element of disabling a precharge operation when data are written in the next memory access cycle nor of incurring a memory performance penalty to reduce power dissipation associated with bitline precharge operations. Therefore Tanaka does not anticipate every element of Applicants' claimed method and memory array. Claims 2-7 depend from claim 1 and new claim 12 depends from claim 10, respectively. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 1-7 and 11 under 35 U.S.C. § 102(b) has been overcome.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 9 and 10, stating that such claims would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Applicants respectfully submit that claims 9 and 10 have been amended to include all the limitations of the base claim and any intervening claims to overcome the Examiner's objection and are therefore in condition for allowance.

Prior Art Made of Record

The prior art made of record by the Examiner and not relied upon, i.e. Takahashi, et al. (U.S. Patent App. No. 2005/0047239); and Kirihata, et al. (U.S. Patent No. 6,404,689), have been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of pending independent claim 1.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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